REMARKS

Claims 1-45 are pending in the present application. Claims 1, 3, 5, 9-12, 14, 16, 18, 20, 25, 26, 31-33, 35, 36, and 41-44 are amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 112, Second Paragraph

The Office Action rejects claims 11, 12, 31, and 32 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed.

As to claims 11 and 12 and 31 and 32, the Office Action states:

> Each of claims 11 and 12 recites the limitation "the response" in line 1 of claims 11 and 12. There is insufficient antecedent basis for this limitation in the claims.
>
> Claims 31 and 32, each recites the limitation "the response" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claims 1, 11, 12, 30, 31, and 32 are amended to recite a mimicked response to differentiate between a response from the peripheral device and a mimicked response that is sent when the peripheral device does not respond to the request.

Therefore, Applicant respectfully requests withdrawal of the rejection of claims 11, 12, 31, and 32 under 35 U.S.C. § 112, second paragraph.

II. 35 U.S.C. § 103, Obviousness

The Office Action rejects claims 1-45 under 35 U.S.C. § 103 as being unpatentable over Chow (U.S. Patent No. 6,078,742). This rejection is respectfully traversed.

As to claims 1-45, the Office Action states:

> As per claim 1, Chow discloses a method and system for emulating data transfer between a bus device and a memory of a system with feature limitations very similar to the claimed invention. According to Chow, the method includes steps

> detecting a signal on the bus indicating a request to access the device (col. 4, lines 27-46),
>
> monitoring the bus for a response by the device (col. 3, lines 18-45), and
>
> sending a response to the signal within bus cycles for access without a response being made by the device (col. 4, lines 29-46). Chow does not expressly disclose the feature of a selected period of time passes as claimed.
>
> Practitioner in the art at the time of the invention was made would have found Chow disclosure of the bus cycles for the sending of response would imply the limitation of a selected period of time as claimed because bus cycles in computer processing data is to measure clock time interval (a period of time) usually preselected such that the data processing system would take to process data. In other words, bus cycle in the present data processing system has been designed to represent for a preselected time period so that the data processing would process data in a synchronous manner.

Office Action, dated March 19, 2004. Applicant respectfully disagrees. The cited portions of *Chow* state:

> As shown in **FIG. 3**, although from the perspective of software driver routines, a sound card **64** appears to be connected to an Industry Standard Architecture (ISA) bus **68**, the sound card **64** is actually connected to a higher performance Peripheral Component Interconnect (PCI) bus **62**. As typical for older software routines (e.g., DOS-based routines) written for ISA bus devices, the software driver routines set up data transfers between the sound card **64** and a system memory **54** by programming a direct memory access (DMA) controller **70**. However, as typical with PCI bus devices, the sound card 64 accesses the system memory **54** without aid from the DMA controller **70**. To maximize compatibility between the sound card **64** and the software driver routines, the sound card **64** monitors the PCI bus **62** for attempted accesses by the software driver routines to registers of the DMA controller **70**. The sound card **64** emulates the response of the DMA controller **70** to these accesses and extracts information (e.g., memory addresses and the size of the data transfer) needed to perform requested data transfers between the sound card **64** and the system memory **54**. As a result, the sound card **64** accesses the system memory **54** using the PCI bus **62** (i.e, only pseudo DMA channels exist for the benefit of the sound card **64**), and the sound card **64** remains backward compatible with the software driver routines. Furthermore,

> a specialized controller (e.g., a DDMA or PC/PCI controller) in the bridge circuit **60** is not required.

Chow, col. 3, lines 18-45.

> As shown in **FIG. 6**, another group **112** includes registers that might affect the use of the pseudo DMA channel assigned to the sound card **64**. A write operation to one of these registers affects one of the DMA (pseudo or actual) channels. Although the write operation contains an identifier indicating the affected DMA channel, the sound card **64** first claims the write operation to determine which DMA channel is affected. The sound card **64** subsequently rebroadcasts the write operation to the DMA controller **70** The group **112** of registers include master (for the master DMA controller **80**) and slave (for the slave DMA controller **82**) DRQn (wherein the suffix "n" indicates the DMA channel number) request registers which allow software of the computer system **50** to request use of a DMA channel. The group **112** of registers also include master and slave DMA mask registers which allow software to selectively mask the DMA channels. The group **112** of registers further include slave and master DMA mode registers which allows the selection of transfer mode (e.g., demand, single, block or cascade) to be used with a selected DMA channel.

Chow, col. 4, lines 27-46. *Chow* teaches a hardware emulation mechanism that allows a peripheral device connected to a peripheral component interconnect (PCI) bus to emulate the direct memory access (DMA) controller. This allows software drivers for the peripheral device to operate as if the peripheral device is connected to an industry standard architecture (ISA) bus through DMA. When the software driver sends a request to access the peripheral device through DMA, the device on the PCI bus sees the request intended for the registers in the DMA controller that are reserved for a pseudo DMA channel. The peripheral device then sends a response emulating the DMA controller.

In contradistinction, the present invention provides a mimic device in a data processing system for mimicking a peripheral device for use within the data processing system, wherein the peripheral device may be disconnected from a bus. The mimic device detects a signal on the bus indicating a request to access the peripheral device and monitors the bus for a response by the peripheral device. When a selected period of time

passes without a response being made by the peripheral device, the mimic device sends a mimicked response to the signal. Thus, the mimic device allows a peripheral device to be inoperative or disconnected from the bus, while requests may still be directed to the peripheral device.

Chow does not teach or suggest detecting a signal on the bus indicating a request to access the **peripheral** device and monitoring the bus for a response by the **peripheral** device, as recited in claim 1. Rather, the peripheral device (sound card) in *Chow* detects a request to access a register in the DMA controller that corresponds to a pseudo DMA channel and immediately sends a response on behalf of the DMA controller. There is no need in *Chow* for the peripheral device to monitor for a response from the DMA controller, because a response is not expected when a request corresponds to the pseudo DMA channel. It follows that, while the peripheral device in *Chow* does emulate a response of the DMA controller, there is no need whatsoever to do so when a selected period of time passes without a response being made, as recited in claim 1, because no response will be made by the DMA controller in *Chow* regardless of the period of time selected.

The applied prior art fails to teach or suggest each and every claim limitation, particularly as amended, even as modified in the Office Action. Therefore, *Chow* does not render claim 1 obvious. Independent claims 14, 18, 27, 30, 35, and 41 recite subject matter addressed above with respect to claim 1 and are allowable for the same reasons. Since claims 2-13, 15-17, 19-26, 28, 29, 31-34, 36-40, and 42-45 depend from claims 1, 14, 18, 27, 30, 35, and 41, the same distinctions between *Chow* and the invention recited in claims 1, 14, 18, 27, 30, 35, and 41 apply for these claims. Additionally, claims 2-13, 15-17, 19-26, 28, 29, 31-34, 36-40, and 42-45 recite other additional combinations of features not suggested by the reference.

More particularly, with respect to claim 2, the Office Action states:

> As per claim 2, Chow discloses the bus is a small computer system bus interface (Figs. 4, 9).

Office Action, dated March 19, 2004. Applicant respectfully disagrees. The cited figures of *Chow* are as follows:

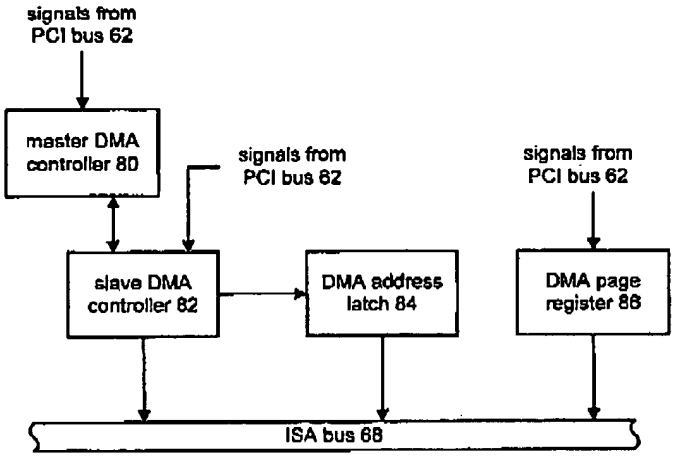

FIG. 4

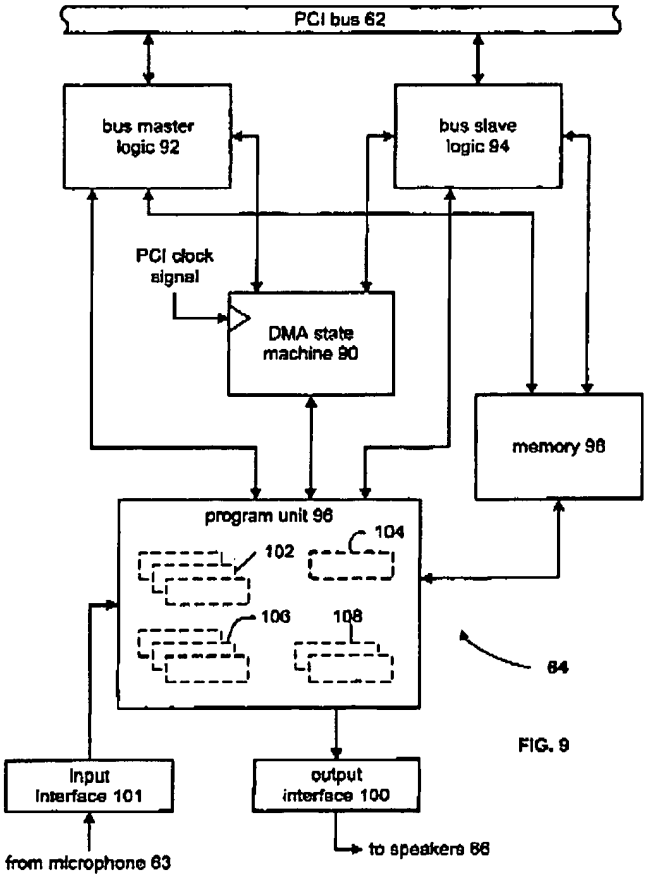

FIG. 9

Neither of the cited figures shows a small computer system bus interface. In fact, the term "small computer system interface" and the acronym "SCSI" appear nowhere in the reference. As such, *Chow* does not teach or fairly suggest each and every limitation of claim 2 and, thus, does render claim 2 obvious. Claims 15, 19, 28, and 34 recite subject matter addressed above with respect to claim 2 and are allowable for the same reasons.

With respect to claim 4, the Office Action states:

> As per claim 4, Chow discloses bus busy signals.

Office Action, dated March 19, 2004. Applicant respectfully disagrees. Strangely, the word "busy" does not appear anywhere in the reference. Applicant requests the Examiner point out exactly where in the Chow patent the feature of claim 4 is taught. Applicant submits that Chow does not teach or fairly suggest the feature of mimicking a response by a peripheral device by sending a busy signal. Claims 17, 21, 29, 31, and 37 recite subject matter addressed above with respect to claim 4 and are allowable for the same reasons.

With respect to claim 9, the Office Action states:

> As per claim 9, Chow discloses the device would not be present in the data processing system (Figs. 4 and 9).

Office Action, dated March 19, 2004. Applicant respectfully disagrees. It is unclear what is allegedly absent from these figures. **Figure 4** is a block diagram showing the direct memory access controller of **Figure 3**. **Figure 9** is a block diagram showing the sound card of **Figure 3**. Therefore, both the sound card and the DMA controller or *Chow* are present in **Figures 3, 4, and 9**. Chow fails to teach or suggest emulating a device that is not present in the data processing system, as recited in claim 9. Claim 25 recites subject matter addressed above with respect to claim 9 and is allowable for the same reasons.

With respect to claim 43, the Office Action alleges that Chow teaches starting a timer for emulation in Figure 10. The cited figure of *Chow* is as follows:

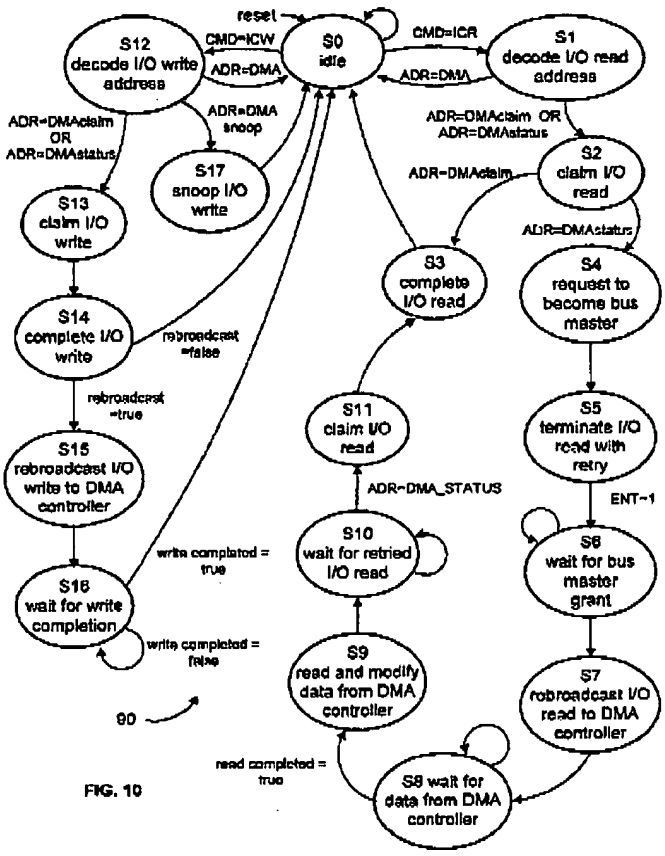

FIG. 10

Neither the cited portion nor any other portion of *Chow* even mentions starting a timer. In fact, the word "timer" appears nowhere in the reference. Applicant submits that *Chow* does not teach or fairly suggest that ascertaining that a device is to be mimicked comprises starting a timer. Rather, *Chow* teaches that a response by the DMA controller is to be emulated only when the registers corresponding to a pseudo DMA channel are accessed. Chow fails to teach or suggest each and every claim limitation; therefore, Chow does not render claim 43 obvious.

Therefore, Applicant respectfully requests withdrawal of the rejection of claims 1-45 under 35 U.S.C. § 103.

III. Conclusion

It is respectfully urged that the subject application is patentable over the prior art of record and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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